Electrical and Structural Characteristics of Strained - Si MOS Structures as a Function of Strained-Si Overlayer

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Strained-Silicon (s-Si) has already been applied to CMOS technology. The study of the structural and electrical properties of s-Si MOS (Metal-Oxide-Semiconductor) structures with ultrathin gate dielectrics is important, especially as a function of the strained–Si overlayer thickness, where a variety of phenomena remains under investigation [1]-[2]. This is the aim of the present work. For this purpose, ultrathin oxides formed in 100% N_2O ambient are used as gate dielectrics. Si oxynitridation in N_2O ambient leads to the formation of ultrathin oxides at high temperatures [3], thus enabling a parallel study under high thermal budget conditions.

The strained-Si structures examined herein consist of either a 27.5 nm thick s-Si overlayer epitaxially grown on a relaxed constant composition $Si_{0.9}Ge_{0.1}$ substrate (S1) or a higher-strain 13 nm s-Si overlayer on a $Si_{0.78}Ge_{0..22}$ substrate (S2). In order to study the effect of the overlayer thickness, certain structures were chemically etched using a modified RCA solution. Oxynitridation has been performed at temperatures of 800 – 900 ^{0}C for various time intervals. Raman spectroscopy and Transmission Electron Microscopy (TEM) have been used in order to study strain preservation and the remaining s-Si overlayer thickness after the etching and oxidation processes. SIMS analysis was performed in order to measure Ge diffusion effect towards the SiO_2/Si interface. Electrical characterisation is performed on Al-gate s-Si MOS capacitors. In the case of thick (>10 nm) s-Si overlayer, C-V characteristics (Figure 1) show a minor frequency dispersion effect, an indication of a very small density of interfacial traps (estimated at $2 \cdot 10^{10}$ $eV^{-1}cm^{-2}$ by the conductance method). In parallel, Raman spectroscopy measurements (Figure 2) indicate strain preservation under the high thermal budget conditions of the oxynitridation process.

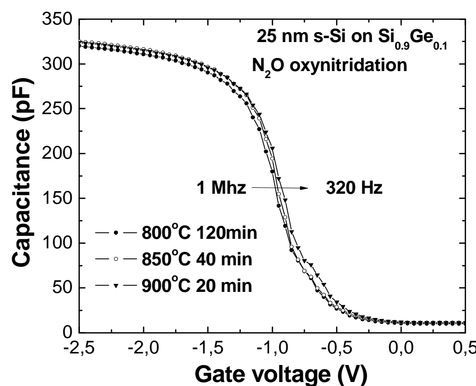

Figure 1: *C-V characteristics of a s-Si MOS structure with 4 nm SiO_2 and 25 nm s-Si overlayer on relaxed $Si_{0.9}Ge_{0.1}$*

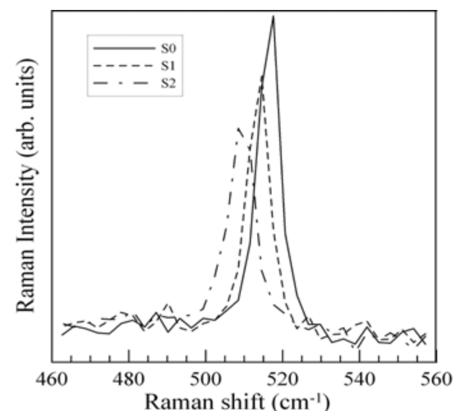

Figure 2: *Raman shifts of s-Si/$Si_{0.9}Ge_{0.1}$ (S1) and s-Si/ $Si_{0.78}Ge_{0..22}$ (S2) MOS structures with equal oxide thickness (4 nm). The s-Si overlayer is 25 and 11 nm respectively. Oxidation was performed at 900^{0}C for 20 min. Raman spectrum of reference bulk Si (S0) is also included.*

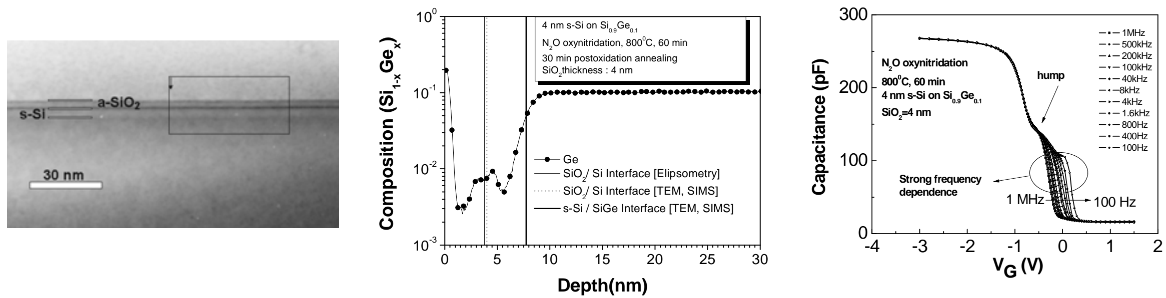

Figure 3: *Ge distribution and C-V characteristics of a s-Si MOS structure with 4 nm SiO_2 and 4 nm s-Si overlayer on relaxed $Si_{0.9}Ge_{0.1}$*

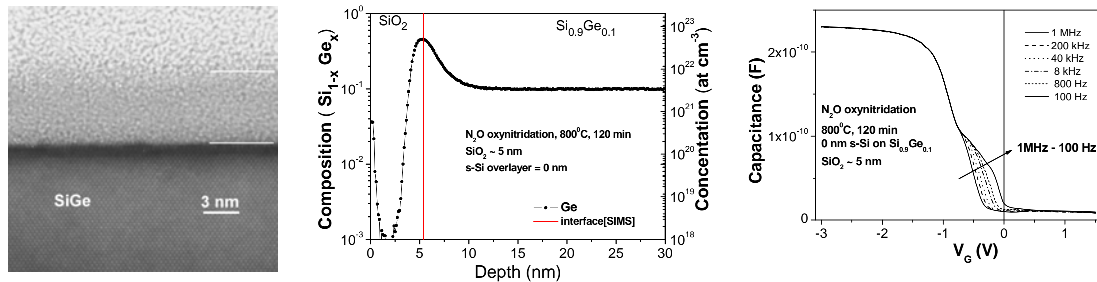

Figure 4: *Ge distribution and C-V characteristics of a MOS structure with 5 nm SiO_2 and no s-Si overlayer on relaxed $Si_{0.9}Ge_{0.1}$*

When the s-Si overlayer is reduced below 5 nm (Figure 3) Ge diffusion from the $Si_{1-x}Ge_x$ layer and segregation at the SiO_2/s-Si interface takes place. In this case, the C-V measurements show a characteristic hump in the depletion and weak inversion regions and a significant frequency dispersion effect in the region of the hump, an indication of high density of interface traps. For this structure, the density of interface traps is estimated at approx. $1x10^{12}$ eV^{-1} cm^{-2} using conductance over frequency measurements. Fixed oxide charge density is estimated at $4.3x10^{11}$ cm^{-2}.

When the s-Si overlayer is eliminated, through over-etching and prolonged oxynitridation processes, a strong Ge pile-up at the $SiO_2/Si_{1-x}Ge_x$ interface takes place (Figure 4). C-V measurements show that the characteristic hump and frequency dispersion effects weaken. For the structure of Figure 4, the density of interface traps is estimated at $5.9x10^{11}$ eV^{-1} cm^{-2} and fixed oxide charge density is estimated at $1.3x10^{12}$ cm^{-2}.

Examining the effect of s-Si thickness, we observe an increased interface trap and fixed oxide charge density when the initial s-Si overlayer is decreased. This is generally attributed to the Ge diffusion and pile-up at the s-Si/SiO_2 interface [1]. In contrast, when eliminating the s-Si overlayer, the interface trap density is significantly reduced, although the Ge pile-up phenomenon is strong. Thus, the higher interface trap density of the samples with less than 5 nm s-Si overlayer compared to those with no s-Si overlayer, originates from defects at or near the *s*-Si/$Si_{1-x}Ge_x$ interface. Since both interfaces are only a few nanometres apart, they both contribute to the density of interface traps. When the s-Si overlayer is removed through over-etching and prolonged oxynitridation processes, a Ge-rich Silicon area is formed instead of an abrupt and well-defined hetero-interface, resulting in the reduction of frequency dispersion phenomena and in less apparent density of interface traps. Similar results are obtained for S2 substrates.

These results clearly indicate that the two existing interfaces of the strained-Si layer, SiO_2/s-Si and s-Si/ $Si_{1-x}Ge_x$, contribute in parallel to the measured interface trap density of ultrathin s-Si layers. In addition, the buried strained-Si/ $Si_{1-x}Ge_x$ interface constitutes a major source of the high density of interface traps measured.

[1] G.K.Dalapati, S.Chattopadhyay, K.S.K.Kwa, S.H.Olsen, Y.L.Tsang, R.Agaiby, A.G.O'Neil, P.Dobrosz and S.J.Bull, IEEE Trans.El.Dev., **53(5)**, p.1142,(2006).

[2] L.K. Bera , S.Mathew, N. Balasubramanian, C. Leitz, G. Braithwaite,F. Singaporewala, J. Yap, J. Carlin, T. Langdo, T. Lochtefeld, M. Currie,R. Hammond, J. Fiorenza, H. Badawi, M. Bulsara, Thin Solid Films , **462–463**, p. 85– 89, (2004).

[3] E. P. Gusev, H.- C. Lu, E. L. Garfunkel, T. Gustafsson, M. L. Green, IBM J. Res. Develop., **43(3)**, p.265, (1999).