The role of gate width in transistor performance: Effects of gate sidewall roughness

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Statistical variability of transistor characteristics has become a major concern associated with CMOS transistors scaling and integration. For conventional bulk MOSFETs, the main sources of the statistical variability are the randomness of discrete dopants, the gate sidewall roughness (usually called line edge/width roughness (LER/LWR)) and the granularity of Poly Gate [1]. In this paper, we focus on the impact of LWR on transistor performance (see schematic view in Fig.1a). The aim is to reveal the role of the transistor gate (channel) width on it, which up to now has been overlooked.

The continuing shrinking of the transistor gate length is accompanied by the scaling down of the gate widths. This scaling down has two implications on LER/LWR impact on transistor performance which are usually neglected in the conventional approach to the problem. The first is that the most commonly used LER/LWR metric, 3rms (sigma) value of sidewall edge points, depends on the line length L included in the measurement process, and decreases as L goes down (see solid line in Fig.1b) [2,3]. This dependence becomes more intense when $L<10\xi$ (with ξ the correlation length) while for low L 3rms $\sim r^{\alpha}$, where α is the roughness exponent of the line morphology. Transferred to gate terminology, this finding means that for gate widths lower than $\sim 10\xi$, the 3sigma value of Gate Length Roughness (GLR) depends on the gate width, apart from its material and process dependencies. Given that $\xi \sim$10-30nm, the above gate width dependence applies for transistors with gate widths lower than 300nm. The second implication is also related with a LWR metrological finding of last years considering the variation of the CDs of line segments of length L [3]. According to it, the decrease of LWR with L is associated with an increase of the CD variation of line segments so that the sum of their squares remains unaltered. In gate terminology, this finding means that the CD variation among the transistors with the same gate width increases as gate width becomes smaller contrary to the behavior of GLR. This is shown in Fig. 1b with the dashed line.

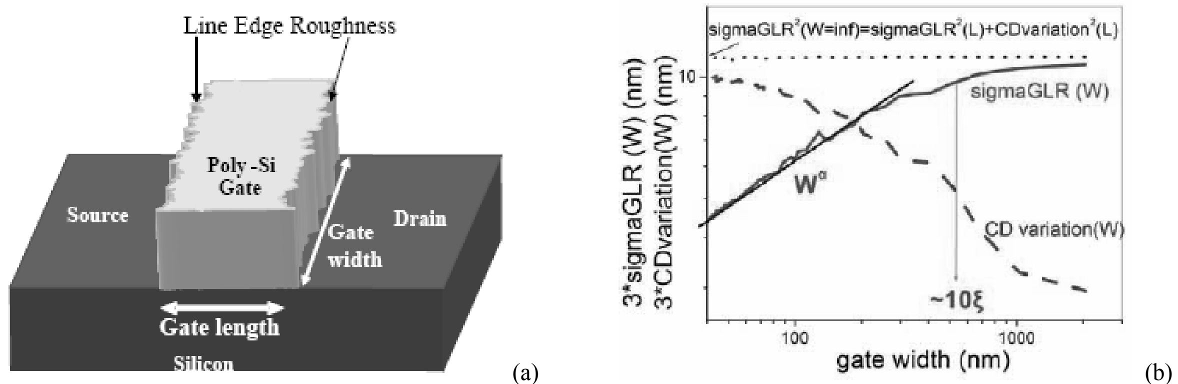

Fig.1. a) Schematic view of a transistor with Line Edge and Line Width Roughness and b) The mean sigma value of GLR (solid line), the CD variation among gates (dashed line) and the sum of their squares (dotted line) versus the gate width W. Notice that as gate width decreases sigma decreases, CD variation increases and the sum of their squares remains fixed to the sigma of GLR with infinite (very large) gate width.

Thus, GLR is not affected alone by the materials of gate stack and the applied processes for transistor formation (lithography and etching steps) but also by a basic design parameter, the gate width. Furthermore, this dependence is controlled by the spatial roughness parameters, the correlation length ξ and the roughness exponent α. In the following, we will examine the effects of ξ,α for fixed W and of W for fixed ξ,α on the statistical variability of transistor performance.

The methodology we employ has been explained elsewhere [4,5]. It is based on modeling both LWR and GLR with fractal self-affine lines characterized by the triplet of roughness parameters (rms value sigma, ξ, α) and also modeling the effects on transistor performance by using the 2D approach proposed by Oldiges [6] in which the

transistor is considered a stack of 2D ultra-small transistor with no roughness.

Fig. 3a shows the effects of , on the mean value of threshold voltage shifts V_{th} from the nominal (no roughness) value for fixed gate length CD=45nm and gate width W=135nm. The transistor gates that have milder degradation effects on the device electrical performance (smaller absolute values V_{th}) are those with low and values. Also, Fig. 3a shows that correlation length affects more drastically transistor electrical characteristics than the roughness exponent . Thus, the conclusion here is to seek changes in resist and/or process properties that lead to lower values of all LWR/GLR parameters.

In Fig. 3a we kept the gate width invariant W=135nm. However, the transistors employed in IC may have a spectrum of gate widths W. Fig. 3b quantifies the effects of gate width variations on threshold voltage shift. It shows the curves $F_{gt}( )$ for varying W (90,135 and 180nm), keeping this time fixed the sigma(W=inf)=2nm, the gate length L=CDnom=45nm and the roughness exponent =0.5. The yield F_{gt} is defined as the fraction of transistors F_{gt} with gate voltage thresholds $0.90\ V_{gth,ideal} < V_{gth,i} < 1.10\ V_{gth,ideal}$.We deduce that the beneficial effect of correlation length reduction remains unaltered for all gate widths W. Furthermore, we find that for fixed CD and GLR parameters [sigma(W=inf), ,] the yield gets higher values as W increases.

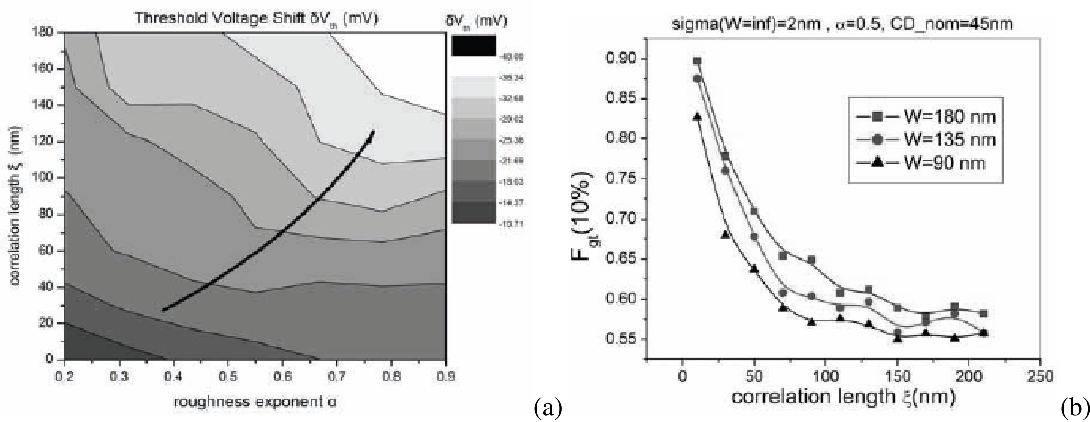

Fig. 2. a) Dependence of the average threshold voltage shift V_{th} on the spatial GLR parameters , for fixed W=135nm and sigma=2nm. The arrows show the directions for increasing the absolute values of shifts V_{th}. Modeling predicts that lower , are more beneficial with respect to GLR effects on threshold voltage deviations. b) Dependence of the transistor yield F_{gt} for various W as a function of keeping fixed sigma=2nm and =0.5.

We have also investigated the effects on the average and standard deviation of the off state leakage currents. It has been found that both estimated quantities (average value and standard deviation) decrease as we move to lower , . Furthermore, it seems that the roughness exponent has more drastic effects on the average value rather than the correlation length. This differentiates the average off current behavior than that of the standard deviation and of threshold voltage shifts and deviations.

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